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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Ratner & Prestia
One Westlakes Berwyn
PO Box 980
Valley Forge, PA 19482-0980

EXAMINER
TANG, KENNETH

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/489,652	BURROUGHS ET AL.
	Examiner	Art Unit
	Kenneth Tang	2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4 and 8-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 8-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the Amendment on 6/14/04. Applicant's arguments have been fully considered but are now moot in view of the new grounds of rejections.

2. The Examiner has acknowledged that claims 1 and 5-7 have been cancelled. Claims 2-4 and 8-26 are now presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "off-core and memory-mapped registers" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. Claims 2-4 and 8-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

a. In claim 9, "a register and an edge detector both coupled between the first and second processors" is indefinite because it is not understood how a register can be coupled between (located outside) the two processors when a register, by definition, is a storage area located within the processor. In addition, "a register and an edge detector both coupled between the first and second processors" is indefinite because it is not made explicitly clear if there are one or two of each registers and edge detectors to enable coupling between both processors. In Applicant's Fig. 4, it is shown that a first register (44) is coupled to the first processor (41) and a second register (49) is coupled to the second processor (46). Likewise, a first edge detector (45) is coupled to the second processor (46), and a second edge detector (48) is coupled to the first processor (41).

b. Claims 14 and 20 are rejected for the same indefinite reasons as the rejection of claim 9 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2-4 and 8-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 3,896,418) in view of Milton et al. (hereinafter Milton) (US 4,862,452).**

6. As to claim 9, Brown teaches a system for providing an interrupt signal comprising

a data bus coupled to the first processor for routing parallel bits of data *(Fig. 3a)*,

a register and an edqe detector both coupled between the first and second processors *(col. 62, lines 7-10 and 42-43, col. 30, lines 13-29)*,

the register coupled to the data bus for storing the parallel bits of data, at least one of the parallel bits of data having an active logic level *(col. 6, lines 38-63, col. 7, lines 45-56 and Abstract)*,

the edge detector coupled to the register for detecting active logic levels stored in the register and converting each active logic level into an interrupt signal *(col. 62, lines 7-19, col. 30, lines 13-29)*, and

7. Brown does teach having an edge detector coupled to an interrupt terminal for interrupt signals *(col. 62, lines 7-19, col. 30, lines 13-29)* but Brown fails to explicitly teach providing an interrupt signal routed from a first processor to a second processor. However, Milton teaches a communication system between digital signal processor (DSP) modules controlled by a main

controller (router) providing the interrupt signals *(col. 1, lines 27-42 and 61-68, col. 2, lines 21-25 and 44-63)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of providing an interrupt signal from a first processor to a second processor to the existing system of Brown in order to increase the functionality of data communication and allow more features in data communication *(col. 1, lines 8-11 and 27-42)*.

8. As to claim 10, Brown teaches wherein the register includes a first set of flip/flops, each flip/flop storing one of the active logic levels, and the edge detector includes a second set of flip/flops, each flip/flop detecting one of the active logic levels *(Fig. 29)*.

9. As to claim 11, Brown teaches further including an address bus coupled between the first processor and the register, and a predetermined address for the register, wherein the first processor routes the parallel bits of data to the register by setting the predetermined address on the address bus *(see Abstract)*.

10. As to claim 12, Brown teaches wherein the register is an off-core register and is enabled by a write strobe signal system from the first processor *(see Claim 6 and col. 5, lines 1-18)*.

11. As to claim 13, it is rejected for the same reasons as stated in the rejection of claim 9.

12. As to claim 14, it is rejected for the same reasons as stated in the rejection in claim 9.

13. As to claim 15, it is rejected for the same reasons as stated in the rejection of claim 10.

14. As to claim 16, it is rejected for the same reasons as stated in the rejection in claim 9.

15. As to claim 17, it is rejected for the same reasons as stated in the rejection of claim 4.

16. As to claim 18, Brown teaches further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register *(see Abstract)*.

17. As to claim 19, Brown teaches wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and the interrupt signal is enabled for a duration of a clock cycle *(col. 7, lines 15-30)*.

18. As to claim 20, it is rejected for the same reasons as stated in the rejection of claim 9.

19. As to claim 2, Brown teaches wherein the register is a memory mapped register *(col. 11, lines 29-41)*.

20. As to claim 3, Brown teaches data exchanges between multiple DSPs using an off-core and memory-mapped registers *(col. 9, lines 12-28, col. 11, lines 11-28)*.

21. As to claim 4, it is rejected for the same reasons as stated in the rejection of claim 9.

22. As to claim 8, Brown teaches the method including the steps of enabling the register during a write cycle, and storing the parallel bits of data when an address of the register matches a predetermined address *(col. 41, lines 1-9)*.

23. As to claim 21, it is rejected for the same reasons as stated in the rejection of claim 10.

24. As to claim 22, it is rejected for the same reasons as stated in the rejection of claim 16.

25. As to claim 23, it is rejected for the same reasons as stated in the rejection of claim 4.

26. As to claim 24, it is rejected for the same reasons as stated in the rejection of claim 9.

27. As to claim 25, it is rejected for the same reasons as stated in the rejection of claim 18.

28. As to claim 26, it is rejected for the same reasons as stated in the rejection of claim 19.

Response to Arguments

29. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the invention uses **active bits from a single data word** as interrupt signals that may be routed to interrupt terminals of a second processor. This advantageously reduces the number of dedicated output terminals required in the first processor, because the need for dedicated interrupt signal outputs are eliminated") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

30. Applicant's arguments in regards to claims 9, 14, and 20 have been fully considered but are now moot in view of the new grounds of rejections.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt
9/10/04

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100